WAVECREST Corporation

ACHIEVING ±30PS ACCURACY IN THE ATE ENVIRONMENT

Application Note No. 114

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Introduction

Most IC manufacturers have purchased digital or mixed signal LSI or VLSI ATE systems within the last one to four years. These systems have overall timing accuracies of from ±500ps to ±3.0ns and the latest ATE systems are quoting ± 350ps overall accuracies. Also, most, if not all, of the new Pentium® clock drivers and new LAN/Telecom devices specify PLL propagation and jitter measurements in the sub 100ps range.

These devices require less than ±50ps to ±250ps clock skew with guaranteed jitter specifications of less than 15ps specified on a cycle by cycle basis. Serial LAN, telecom mixed-signal devices also require accurate jitter and propagation delay testing in the order of 100ps or less.

This note offers various techniques for interfacing LSI/VLSI ATE to external time measurement instruments for making extremely accurate propagation delay and jitter measurements with accuracies on the order of ±30ps and noise floors of less than 5ps.

Scope

The economic and technical benefits of extending the capability of current ATE with external instrumentation is not well documented. Yet this note outlines several techniques to extend the useful life of the IC manufacturers' existing ATE systems for making precision time and jitter measurements. Even today, many of the latest ATE systems on the market do not possess this capability.

ATE jitter caused by system and DUT noise up at the load board makes accurate jitter measurements on high frequency PLL clock drivers for Telecom, Pentium® and disk drives almost impossible. Using a truly differential time measurement system eliminates measurement jitter generated by the ATE system for all but period measurements. Also, systematic or non-Gaussian jitter distributions of the ATE system distort DUT jitter distributions, thereby giving false results.

Another problem associated with digital testers is accurate period measurement of devices with random PLL-driven outputs. Outputs can be programmed to frequencies not synchronous with the ATE clock. Test times can become very long when trying to test these types of outputs with a synchronous test system. External instruments can differentially measure any of these outputs asynchronously with respect to the ATE system timing, but are usually slow, and hard to program and interface into the ATE environment.

In a digital ATE, a strobe search is used to measure propagation delays. In mixed signal testers, undersampling or waveform digitizing is often used for time measurement. Both are slow due to the iteration algorithms necessary to make the measurement. They are limited by LSB resolutions in the tens to hundreds of picoseconds. The strobe search routine works poorly with nonsynchronous pulses and does not provide jitter information. Then again, some ATE systems have built-in differential time measurement capability but are plagued with high jitter noise floors and specifications that preclude making less than ±100ps timing measurements.

Accuracy Considerations

When greater accuracy is required, an external instrument is often the solution. Interfacing this instrument in a noisy ATE environment to make propagation delay measurements with 50ps accuracy and jitter measurements of less than 5ps is not a trivial matter.

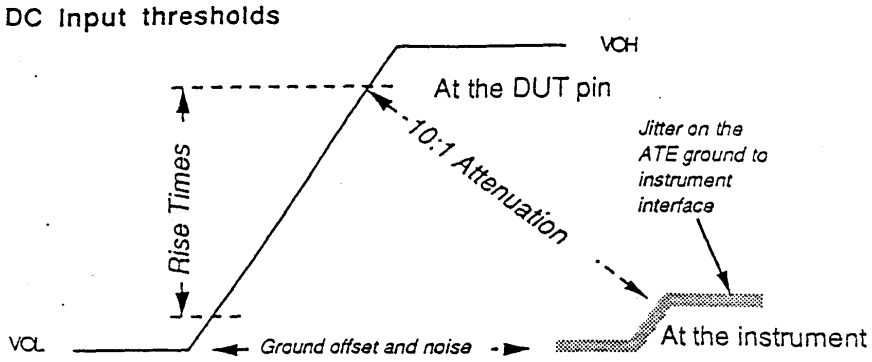
Selecting the proper DUT interface solution requires understanding the requirements of the DUT technology being tested. Refer to the IC manufacturers data book and system design handbooks for interface and test criteria required by the device being tested.

Interfacing the DUT to the ATE system through a test socket, handler or wafer prober is usually the first challenge. The *di/dt* of the device output signal and the number of output pins usually determines the size of an interface problem. Today, multilayer interface boards are common place, yet interfacing to the handler or wafer prober can seriously degrade signal rise times and inject noise that causes high jitter and incorrect readings in the sub 1/4 nanosecond range.

Devices such as ECL and GaAs require terminated environments where pull up and/or pull downs are required. While CMOS and TTL, because of bidirectional busing, usually require back termination for high-speed edges. (See reference 1 for back match modeling information.)

The following parameters are important when considering the need for an external time measurement instrument:

1. DUT load board interface scheme
2. Instrument one-shot resolution/accuracy
3. Instrument DC input threshold accuracy
4. Instrument physical location/installation
5. Instrument jitter noise floor
6. Instrument throughput over data interface
7. ATE to instrument Arming/Trigger modes
8. Bandwidth required to reproduce Tr/Tf of DUT



Input Attenuation used to achieve high bandwidth increases input errors due to DC voltage reference and instrument to ATE ground offsets.

A high ATE system jitter noise floor masks real DUT performance. Most ATE systems specify 20ps to 50ps rms jitters. For Telecom work rms jitter must be multiplied by 6 to 8 to get 6 to 8 sigma results. That means the ATE system at 50ps rms jitter is really 300ps to 400ps of peak-to-peak jitter! Consequently, for such measurements an instrument with 5ps rms jitter or less is necessary.

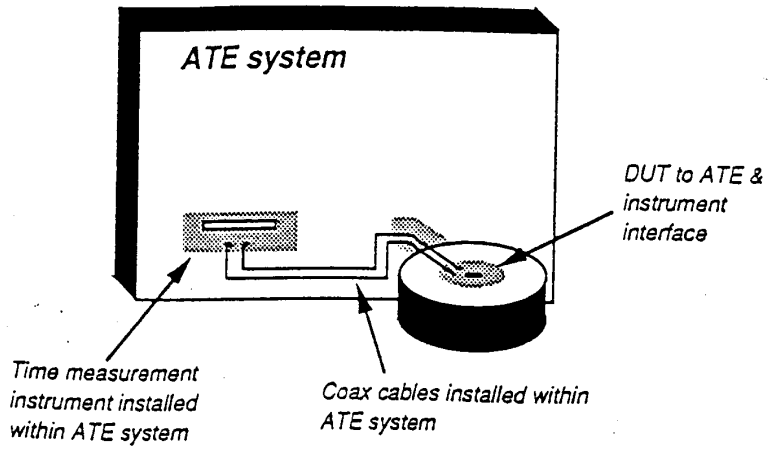
An interface that induces crosstalk, ground bounce, and impedance glitches or does not match the device output impedance properly, does not test the DUT to repeatable specs and may create more problems than it solves. Measurement jitter caused by ground-to-ground noise can be in the hundreds of millivolts if the instrument is not properly connected to the ATE test head. Ground loops through the line cord and safety ground connection may need to be isolated to eliminate this problem. These problems are usually related to 60-cycle noise and can be visually diagnosed with an oscilloscope.

When attenuation is used at the DUT interface for increased bandwidth, high DC threshold resolution and accuracy is required. In the case of a 10:1 attenuation, 1mV to 5mV of reference resolution at the instrument inputs translates to 10 to 50mV of resolution at the DUT pin.

Front-end DC offset and gain errors translate to timing accuracy and repeatability errors. In the above example, a 1nS rise time, 5-volt amplitude pulse would translate to a ±22ps reference error at the instrument. An ECL or GaAs IC at 400ps rise time, 8OOmV amplitude, would see ±42ps of timing error. It's hard to achieve ±30ps overall timing accuracy with many DC probing errors.

Also, up to 5mV of DC ground reference shift can occur between the instrument and ATE system. And, AC noise can also appear across the same coax ground shield to the tune of ±20mV peak to peak.

The ATE environment



LSI and VLSI ATE systems normally have room within the confines of the system cabinets for external instruments. Most of these systems also have high quality 50Ω coax cables running between the instruments and test-head load-board interface hardware. Some systems have special coax pogo-pins to make contact to the DUT board. This level of integration is recommended for an accurate low jitter production and engineering environment.

Installing the time measurement instrument within the ATE system using a high bandwidth double shielded 50Ω coax interface to the test head is recommended. The length of the cable between the DUT and instrument determines the overall bandwidth of the measurement interface. See reference 5 for information on selecting high quality coax cable and connectors. Also, check to make sure the 60-cycle power line is not inducing hum between the test head and the test instrument. This may occur if the line power was wired from a different circuit. If rewiring is not possible, then route the line cord through a toroid filter to reduce the interference.

A noise-free installation can achieve a high degree of differential accuracy. ±30ps or better is achievable in a clean installation.

Interface Schemes

The proper interface at the load board is required to transfer the signal from the DUT to the time measurement instrument. If possible, use the interface as all or part of the load for the device. This reduces any error the interface may contribute toward measurement accuracy and repeatability.

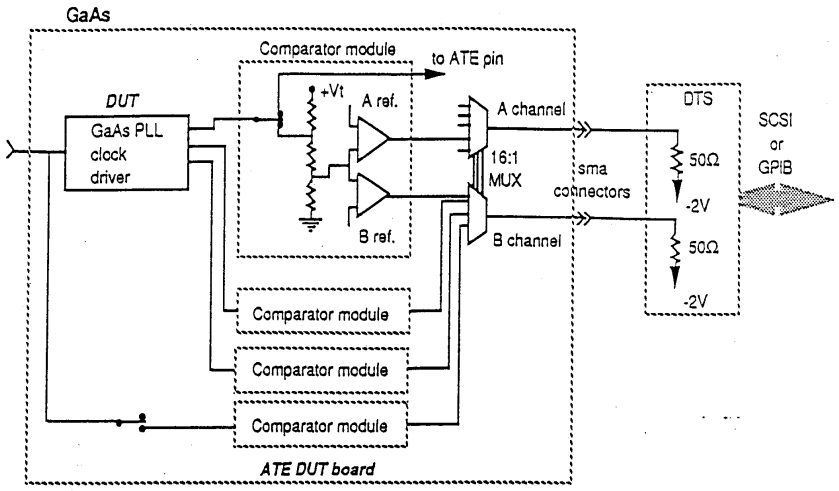


Figure 1.

Digital Gallium Arsenide devices most commonly fall into two main categories: ECL-compatible devices that work in the same terminated environment as ECL devices, and other. Other means non-ECL swings and levels. Some can be positive and some negative. Some swing less than one volt, while others swing three to five volts. Follow the manufacturer's recommended termination voltage and loading scheme. Generally, because of the high edge rates, GaAs is always used in an end-of-line termination scheme.

The interface shown in figure 1 uses resistive pull-ups and pull-downs. It places ECL comparators and a MUX driver on the DUT load board to eliminate the need for an external relay matrix and the associated coax cables. This implementation requires only two 50 ohm coax cables extending from the DUT board to the external time measurement instrument.

This example enables the user to use a low cost or older ATE system to guarantee clock driver PLL devices with less than 250ps of pin-to-pin skew and clock jitters of less than 10ps. This production solution provides repeatable results due to the minimum number of interconnects. Eclips® or Eclips Lite® ECL is recommended at the comparator and multiplexer due to its propagation delay stability over a wide range of voltages, temperatures and duty cycles.

For deskewing information on the above interface, see "Deskewing Fixtures" in this note. The comparator/multiplexer technique used in figure 1 measures period, frequency, pulse width, rise and fall times and propagation delay when properly deskewed and generates <1ps of jitter rms on its own.

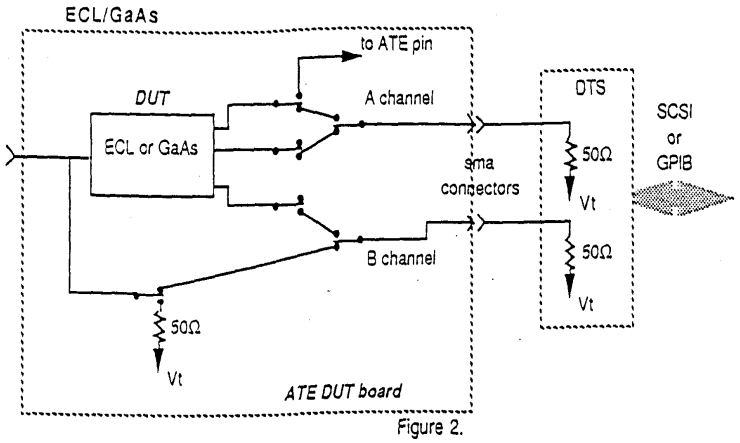


Figure 2.

Current mode ECL and ECL-compatible GaAs are usually resistive terminated (anywhere from 50 to 100 ohms to -2 to +3 volts). The -3 volt devices are called PECL or Positive ECL. Some Telecom SDH clock recovery devices work with all three ECL terminations: -2, ground and +3 volts depending on how they are configured.

External level shifting circuitry can be used to test all modes of such devices. (Refer to reference 5 and 6 for details on shifting ECL and PECL levels.) The solution in figure 2 provides low interconnect capacitance and bandwidth in excess of 1GHz, where low jitter and tight skew measurements are required. COTO series 2900 form 'C' relays were used here to prevent any *stubbing* that can cause reflections. The DTS used for the timing measurements has built-in programmable termination supplies that make level shifting unnecessary.

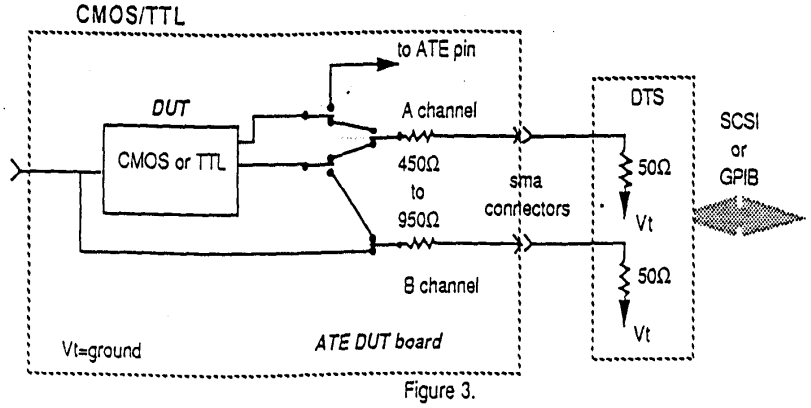


Figure 3.

As previously mentioned, CMOS and TTL devices are usually used in a back-terminated environment because they are designed to be bused or bi-directionally connected. Submicron CMOS devices can achieve greater than 100MHz speeds with rise and fall times of 1ns and faster. Unlike ECL, CMOS is not terminated at the end of the line but back terminated. Back termination is not an ideal environment for accurate time and jitter measurements. Lumped capacitance or impedance variations can obstruct the path from the pin electronics card of the ATE system to the DUT pin; this causes TPD and rise/fall time variations which affects time measurement repeatability. In a back-matched environment, lumped effects manifest themselves more seriously (see reference 5 for details).

Figure 3 shows the CMOS device lines being loaded with the characteristic 500Ω load pull-down. A 450Ω ±1% chip resistor, with low inductance, is placed as close as possible to the OUT output pin or relay. High quality 50Ω coax with high quality connectors, such as SMA, transfer the signal to the time measurement instrument which terminates in 50Ω's This resistor divider arrangement works well to rise times in the 150ps range and provides a 10: 1 voltage divide to the instrument. A 950C resistance can be used in place of the 450Ω resistor if a smaller load is required; then the ratio is 20:1. *For this system to work with good repeatability, the time measurement instrument requires some form of probe DC offset & gain calibration, and input threshold resolution of 100 microvolts or less to compensate for resistor variations and attenuation.* Many bench setups use this same type of probing for time measurement. Consequently, using this technique with the ATE system provides a level of correlation between the two environments.

In figure 4, the CMOS/TTL specifications indicate a pull-up as well as a pull-down resistance or equivalent circuit.

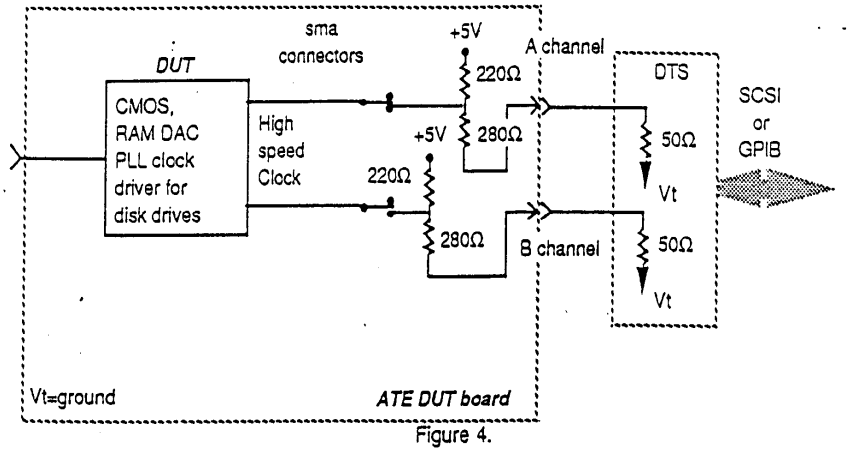


Figure 4.

If required, a relay matrix can be integrated either onto the load board as in figures 2, 3 and 4, or provided externally. High quality relays with bandwidths of 1 to 4GHz are available for these types of applications. Depending upon the device type, anywhere from 2 to 10 relays are required for a PLL driver or clock recovery device.

Features/issues that influence relay selection are size, AC impedance, contact capacitance, relay bandwidth, contact resistance, contact life and gas environment around the relay contacts. Relays sealed in an inherit gas last many times longer than unsealed relays.

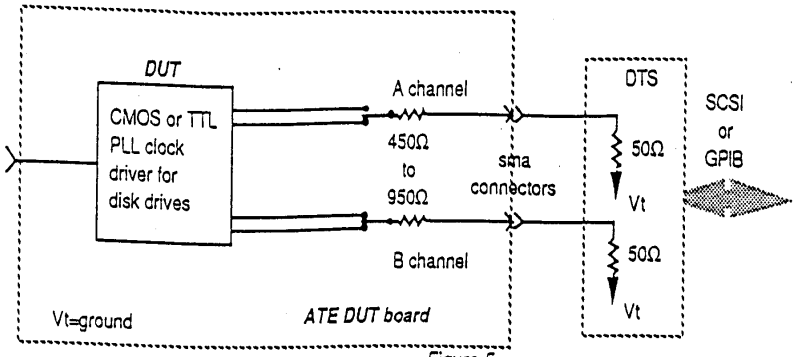


Figure 5.

Figure 5 shows an interface implementation where the external instrument makes the voltage and timing measurements. No connection is made to the ATE system for the PLL clock skew pins. The ATE system provides OUT power and pattern stimulus.

The advantages of interface schemes such as those shown in figures 3, 4 and 5 are: bandwidths on the order of 1 to 3GHZ, low noise, and jitter induced by the interface and skew measurements in the area of ±30ps that are possible if resistor tolerances are held to within 1%.

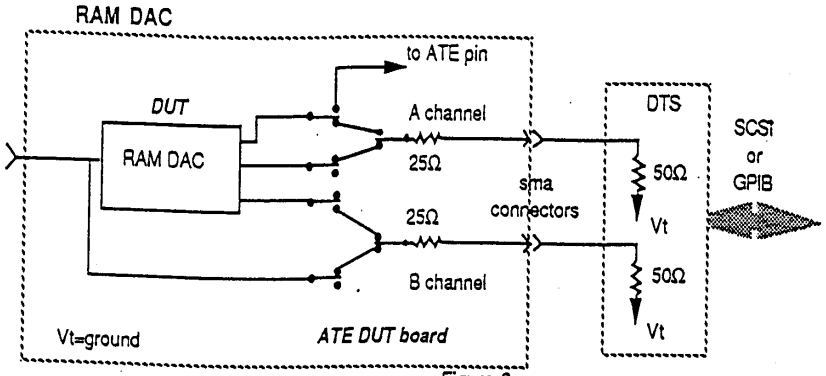


Figure 6.

RAM DAC output pixel drivers are usually current mode designs for speed. This means they require a low impedance termination for proper operation. Most RAM DACs require a 75 ohm resistive termination. Whether, imbedded or not, as the frequency and rise time of the DAC increases, so does the complexity of the interface. A 25Ω low-inductance chip resistor in series with 50Ω coax to the time measurement instrument provides a high bandwidth 75Ω termination. The DC reference voltage scaling factor is 1.5:1.

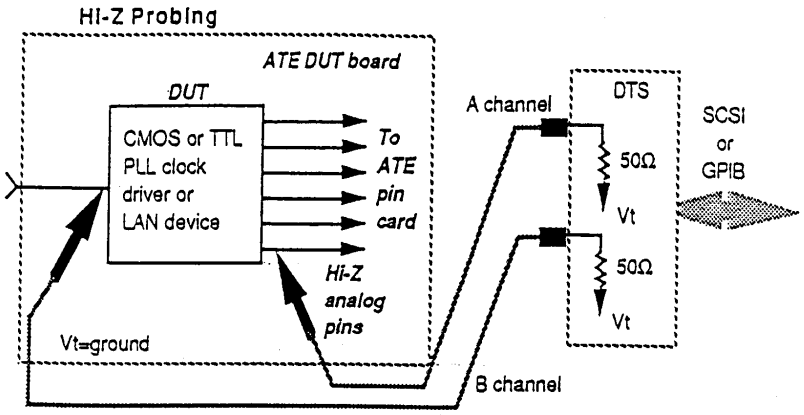


Figure 7.

Active probing may be necessary for devices that cannot tolerate any type of current loading. High voltage swing linear functions with high internal series resistance usually require some form of active interface to buffer the DUT to ATE or external instrument. Refer to references 3 and 4 for details on high impedance active probe design considerations.

PECL logic causes a similar instrumentation interface problem to ECL, one of level shifting without introducing timing or jitter anomalies. The circuit in figure 8 provides a high bandwidth solution for PECL and ECL devices.

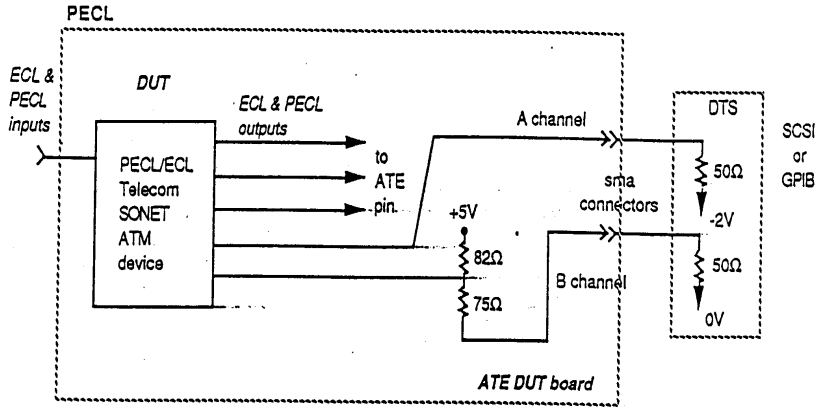


Figure 8.

Figure 8 shows a PECL-to-ground reference level shifter. Chip resistors and capacitors minimize parasitic reactance. High quality 50Ω coax cable is required to transfer signals to the time measurement instrument.

The DC voltage level divide ratio is approximately 2.35:1 with the values shown in figure 8. A typical PECL device VOH and VOL level could be 3.77 Volts and 2.97 Volts. At the instrument, the levels would be 1.57 Volts and 1.23 Volts respectively. Here the IC load and the time measurement instrument probe interface are integrated into one another to reduce the capacitive probing effects of a non-integrated probe. The resistors used here need 1% tolerance and at least 5 times the wattage necessary to reduce thermal drift.

Deskewing Fixtures

No TPD measurements

When only single channel time or jitter measurements are desired, deskewing of the DUT fixture interface to the time measurement instrument is not required. These measurements include: frequency, period, pulse width or rise and fall times, voltage levels and overshoot measurements.

For pulse width measurements, in the case of figure 1 where an active matrix and probe are used, it is necessary to deskew the time it takes the matrix to propagate a leading versus a trailing edge. A pulse of known width is passed down each active path. The resulting measurement is subtracted from the known width and algebraically summed to all future pulse width measurements for each path.

TPD measurements

For all of the interface fixture examples given, the best possible solution for TPD measurements is to insert a chip/IC into the DUT socket with all of its outputs die-bonded together internally, tied to several tester pin driver channels and simultaneously driven. A deskew table for each pin of the DUT and each edge can be measured by the instrument and stored in memory. One pin of the DUT is the "king pin" and a delta table from that pin is generated. Later, this correction factor is only algebraically summed with all future TPD and pulse width measurements. Leading and trailing edge data is required for each comparator in the signal stream. This “deskewing of the interface” need occur only once, when the interface fixture is first fabricated, and then periodically to correct for any drift.

The single biggest issue in using an active matrix is propagating various duty cycles through the matrix to the time measurement instrument. If large variations in duty cycle are to be propagated over the interface then a passive vs. active interface is best. Errors on the order of 50ps to 100ps are possible with duty cycle variations as high as 99%.

Passive interfaces requiring overall accuracies in the 250ps range can easily be deskewed by using the time measurement instrument to measure each path of the DUT interface on the bench, and then entering the results as data correction constants for all fixtures of that type. Deskewing of the coax cables between the interface and the instrument can be done with the techniques provided by the time instrument manufacturer. The *WAVECREST* DTS has built-in firmware and hardware to deskew the DUT interface and coax cables.

Device Output Termination Voltages

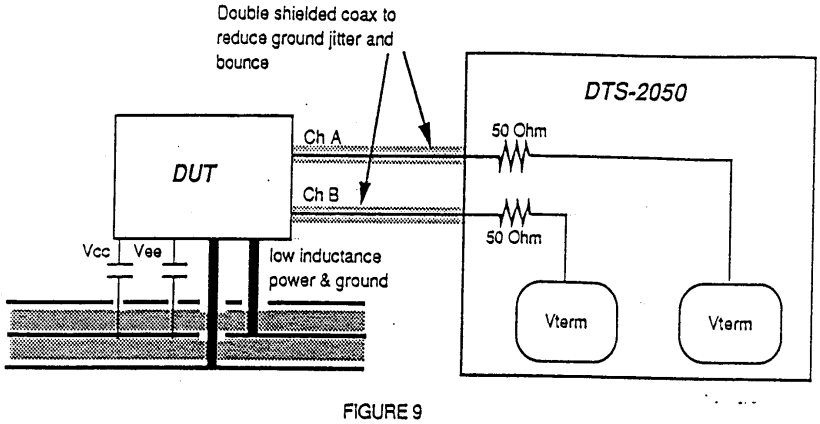


FIGURE 9

The DTS input termination levels are programmable from -3V to +3V. See figure 9. The common mode input operating range of the DTS is shown in figure 10. The input termination resistance is 50-ohms to the termination voltage.

DUT capacitive bypassing is as important as ever. Tr/Tf distortion occurs if any inductance appears between the output termination scheme and the VCC or VEE supplies. The usual .01 µf and 0.1 µf capacitors should be very near the DUT and 1.0 to 40.0 µf of tantalum electrolytic within 1 to 5 inches from the DUT. See reference 2 for high frequency PC layout considerations.

The total self resonant frequency of the bypass: capacitance* and DUT power trace inductance must be greater than the bandwidth required to reproduce the Tr/Tf of the DUT faithfully. If this is not the case, the DUT bypass and power planes require redesign. Instability in the times and jitter can be the result of improper bypassing, which includes the power/ground plane design.

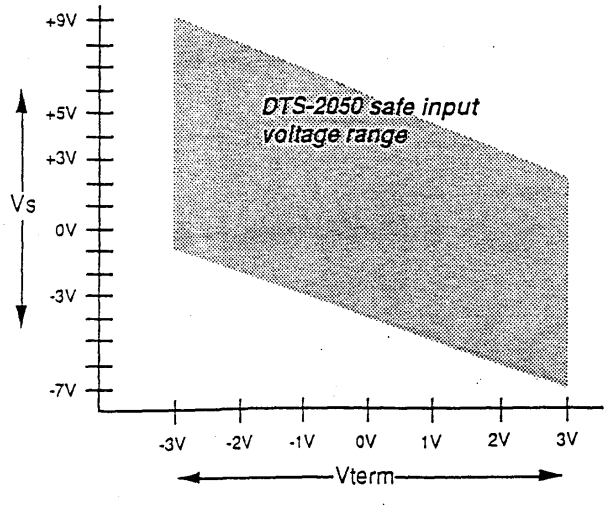


Figure 10

Figure 11 shows the power supply voltage relationships of the DTS to the DUT for GND termination and -2V termination. The safe input compliance of the DTS 2050 is -7V to +3V when the termination supply is set to +3.0 Volts. For PECL logic, use the level shifting scheme shown in figure 8.

Mode	Vcc	Vee	Vterm
GND	+2V	-3V	0V
ECL	0V	-5V	-2V

Figure 11

Conclusions

In the test interfaces described in this note, the Digital Time System (DTS) provides ±30ps of real timing accuracy with jitter noise floors of less than 5ps rms. Attention to all of the following is required to achieve stable and repeatable accuracy.

1. DUT load board interface scheme
2. Instrument one-shot resolution/accuracy
3. Instrument DC input threshold accuracy
4. Instrument physical location/installation
5. Instrument jitter noise floor
6. ATE to instrument Arming/Trigger modes
7. Bandwidth required to reproduce Tr/Tf of DUT

About the Digital Time System

The DTS series of instruments provides precise, high-speed time measurements and is designed for use in ATE and automated lab environments where large amounts of accurate and repeatable data is required.

Because of the *patented* calibration technique used in the DTS design, the linearity and repeatability of all timing measurements can be guaranteed to tight tolerances. Calibration is based on a built in standard with 0.1 femtoseconds of accuracy in 10.0 nanoseconds.

The single-shot hardware resolution of the DTS is 800fs. The high measurement rate of the DTS enables it to take many measurements in a single burst to verity jitter distributions, or to simply verify good continuity on contacts in a production environment.

The input threshold resolution of the DTS 2070 is 100 μV. This enables 1 mV of real resolution at the device through a 10: 1 test probe. DC offset and AC propagation delays of the probes, in the fixture, are calibrated for the utmost repeatability and accuracy.

Programmable voltage termination supplies for each of the DTS inputs enable the testing of ground and -2 volt ECL without special fixtures.

References

Copies of the following references are available upon request from *WAVECREST*, 7275 Bush Lake Road, Edina, MN 55439.

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